Matrix Computations: From Cell Caching to Cell Architectures

Anne C. Elster
elster@computer.org
Dept. of Computer & Info. Science (IDI)
Norwegian Univ. of Sci. & Technology (NTNU)
Trondheim, Norway

Computer architectures are becoming more and more complex. Even COTS (commercial-off-the-shelf) processors now have several types of registers, multiple levels of cache, and more recently multiple cores and features that do not necessarily target computation, but visualization (e.g. the Cell architecture recently announced.)

This presentation will first discuss the indexing technique known as cell caching that was developed by the author back in the early 1990s. The paper will also discuss parallelization issues and the newer techniques behind automatically tuned libraries such as the BLAS library, Atlas. Recent approaches to take advantage of the new multicore cell architectures will also be included.